

# SPECIFICATION

Electronic Version 1.2.8

Stylesheet Version 1.0

## [FABRICATION METHOD FOR SEMICONDUCTOR HOLE]

### Cross Reference to Related Applications

This application claims the priority benefit of Taiwan application serial no. 91112176, filed June 6, 2002.

### Background of Invention

[0001] Field of the Invention

[0002] The present invention relates to the patterning of a semiconductor device. More particularly, the present invention relates to a method for forming a semiconductor hole.

[0003] Background of the Invention

[0004] A prevailing tendency in the semiconductor industry is to reduce the design dimension of the circuitry devices. Photolithography thereby becomes a significant step in the entire semiconductor manufacturing. Anything that is related to the structure of a semiconductor device, for example, the patterning of each layer of thin film, the critical dimension is determined by the photolithography process. In other words, the critical dimension of a device is determined by the advancement of the photolithography technique. Thus, the accuracy in the transferring of a photomask pattern plays an important role. If the transferring of a pattern is not accurate, the tolerance of critical dimension of a wafer is affected to lower the resolution of the exposure light.

[0005]

The proximity effect is a major factor in determining the projection accuracy of a critical dimension onto a wafer surface during the transferring of a mask pattern. The

proximity effect, on one hand, is a form of optical distortion associated with the diffraction of light beams when the light beams are being transmitted through the pattern of a photomask to form images on a wafer. On the other hand, proximity effect is a result from the interference between light beams due to the reflection of light from the substrate of a wafer through the photoresist on the wafer surface. The reflected light, however, would lead to multiple exposures to the photoresist, altering the actual amount of exposure light to the photoresist. This type of phenomenon is especially prominent as the line width approaches the wavelength of the light source. Currently, forming a circular or a elliptical hole employs either the optical proximity correction (OPC) or the 2-in-1 exposure method to resolve the above problem.

[0006] Figures 1A and 2A illustrate the process flow in fabricating a semiconductor hole using the conventional 2-in-1 exposure method. Figures 1B and 2B are cross-sectional views of 1A and 2A along the lines I-I.

[0007] Figure 1A is a schematic diagram illustrating an exposure process, while Figure 1B is a cross-sectional view of Figure 1A along the line I-I.

[0008] Referring to Figures 1A and 1B, a dielectric layer 102 is formed on a substrate 100. A photoresist layer 104 is formed on the dielectric layer 102. Thereafter, a first photomask (not shown in Figure) is used to perform a first exposure to form a pattern on the photoresist layer 104, wherein the pattern formed on the first photomask comprises square patterns. After the pattern on the first photomask is exposed, the pattern is transferred to the photoresist layer 104 forming two diagonally allocated first regions 106. A second photomask (no shown) is then used to perform a second exposure to form a pattern on the photoresist layer 104, wherein the pattern on the second photomask comprises square patterns. Subsequent to exposing the second photomask, the pattern on the second photomask is transferred to the photoresist layer 104, forming two diagonally allocated second regions 108, wherein the two first regions 106 and the two second regions 108 are mirror images.

[0009] Figure 2A is a schematic diagram illustrating a development process, while Figure 2B is a cross-sectional view of Figure 2A along the line I-I.

[0010] Referring to Figures 2A and 2B, the photoresist layer 104 in the first regions 106

and the second regions 108 are removed by means of an exposure process to form holes 110 in the photoresist layer 104, exposing the dielectric layer 102.

[0011] However, in the above method of forming a hole 110 in a photoresist layer 104a, a leakage of light easily occurs during the first exposure and the second exposure. The double leakage of light will easily lead to the formation of a collapsible column 112 (as shown in Figure 1A) located between the diagonally allocated first regions 106 and the diagonally allocated second regions 108. The peeling of the photoresist layer is thus resulted and defects in the dielectric layer in the subsequent process are generated. To prevent the collapse of the photoresist layer, the distance between the holes needs to be controlled. Thus, the pattern density can not be increased and further miniaturization of devices is hindered.

## Summary of Invention

[0012] Accordingly, the present invention provides a method for fabricating a hole in a semiconductor device, wherein aerial image contrast at the edges of the holes in each exposure is increased to prevent the peeling of the photoresist between the holes.

[0013] The present invention provides a method for fabricating a hole in a semiconductor device, wherein the density of holes can increase.

[0014] The present invention provides a method for fabricating a semiconductor hole, wherein the application of optical proximity correction is minimized to simplify the manufacturing process.

[0015] Accordingly, the present invention provides a fabrication method for a semiconductor hole, where the desired elliptical or circular hole pattern is accomplished by performing a first exposure using a first photomask that comprises square patterns that are diagonally allocated. A second exposure is also performed using a second mask that also comprises square patterns that are diagonally allocated. Moreover, the square patterns in the first and the second photomasks are mirror images and are tilted at an angle of 45 degrees.

[0016] The hole pattern for integrated circuits of the present invention is formed with a photomask having a pattern of square patterns that are rotated a fixed angle of 45

degrees. Compare to using two diagonally allocated square patterns that are not tilted as in the prior art, the method of the present invention can increase the aerial image contrast of the opposing edges of each pair of the diagonally allocated holes. The peeling of the portion of the photoresist between the holes is thus prevented. Further, the present invention can increase the density of the hole pattern. Additionally, the standard required by the product design can be achieved during the photolithography of the wafer. The yield and the productivity are thereby increased. The application of optical proximity correction during the photolithography process is thus reduced to simply the manufacturing process.

[0017] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

## Brief Description of Drawings

[0018] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0019] Figures 1A, 1B and 2A, 2B illustrate the process flow for manufacturing a semiconductor hole using a 2-in-1 exposure method according to the prior art;

[0020] Figure 3 is a flow diagram illustrating the process flow for fabricating a semiconductor hole according to one embodiment of the present invention;

[0021] Figure 4 is a top view of the layout of the semiconductor hole formed according to the one embodiment of the present invention;

[0022] Figure 5A is a schematic top view of the contact holes formed for the mask ROM coding process by the conventional 2-in-1 exposure process;

[0023] Figure 5B is a schematic top view of the contact holes formed for the mask ROM coding process by the 45 degree rotation 2-in-1 exposure process of present invention;

[0024] Figure 6 is a top view of the layout of two pairs of diagonally allocated semiconductor holes illustrating the edge of each hole, where the aerial image contrast is increased according to the present invention.

## Detailed Description

[0025] Figures 3 a flow diagram illustrating the process flow for fabricating a semiconductor hole according to one embodiment of the present invention.

[0026] Referring to Figure 3, in step 300, a photoresist is formed on a substrate, wherein the substrate comprises, for example, a semiconductor substrate, a semiconductor device, a conductive layer, a dielectric layer, etc. In one example, step 300 can include forming a semiconductor device on a semiconductor substrate, followed by forming a dielectric layer on the semiconductor substrate to cover the semiconductor device. The dielectric layer is then planarized, followed by forming a photoresist layer on the planarized dielectric layer.

[0027] Thereafter, in step 302, a first exposure is performed using a first photomask that comprises two diagonally allocated polygon patterns, wherein each polygon pattern on the first photomask is rotated a fixed angle from its arrayed position. The photomask of the present invention comprises square patterns, which are exposed to form either circular or elliptical hole patterns. The fixed angle is, for example, best at about 45 degrees since the shortest distance between the two diagonally distributed square patterns that are tilted at an angle of 45 degrees is the greatest, compared to the shortest distance between two horizontally allocated square patterns. Defects formed due to the leakage of light are more effectively reduced to prevent the peeling of the photoresist near the holes after the development process. Defects are further prevented from forming after the performance of the etching process to form the holes.

[0028] After this, in step 304, a second exposure process is conducted using a second photomask that comprises two diagonally allocated polygon patterns that are respectively rotated a fixed angle from their arrayed positions, for example, an angle of 45 degrees. Further, the polygon patterns from the first photomask and the second photomask are mirror images.

[0029] In step 306, a development process is performed to form holes in the photoresist. An ion implantation 308 is performed, for example, for a mask ROM coding process. The purpose of the implant in the mask ROM coding process is to turn off the channel, disconnecting the source region from the drain region. As shown in Figures 5A and 5B, Figure 5A is a schematic top view of the contact holes formed for the mask ROM coding process by the conventional 2-in-1 exposure process, while Figure 5B is a schematic top view of the contact holes formed for the mask ROM coding process by the 45 degree rotation 2-in-1 exposure process of present invention. Moreover, after the contact hole is formed in the photoresist, the photoresist with the hole can be used as a mask to etch the dielectric layer to form contact window in the dielectric layer. Thereafter, the photoresist is removed.

[0030] Beside the ion implantation process described in the above embodiment of the present invention in forming the contact window, the present invention is also applicable to a process for etching circular or elliptical patterns or for forming a via hole.

[0031] To better comprehend the significance of the present invention, please refer to Figure 4, which is a top view of the layout of the hole formed according to the present invention.

[0032] As shown in Figure 4, the photomask pattern 400 of the present invention is a photomask pattern that comprises a plurality of square patterns. The shortest distance between the two diagonally allocated square patterns 404 that are rotated a fixed angle of 45 degrees (represented in solid line) is greater than the shortest distance between the two horizontally allocated square patterns as in the prior art. As a result, as shown in Figure 6, the aerial image contrast of the opposing edges (a vs. b, c vs. d) of each pair of the diagonally allocated contact holes is greatly increased in each exposure. The peeling of the photoresist between the diagonally allocated square patterns due to the leakage of light generated during the exposure process is thus prevented. Moreover, defects that are formed in the patterned dielectric layer in the subsequent etching process are also prevented.

[0033] Based on the foregoing, the present invention uses a first and a second photomasks having two diagonally allocated polygon patterns that are rotated 45

degrees from their arrayed positions to perform two exposures. Compared to the holes that are formed with exposing a pattern having horizontally allocated pattern, the contrast of the optical image between the holes can be greatly increased. Defects resulted from the leakage of light is thus reduced.

[0034] Further, using two diagonally allocated square patterns that are rotated a fixed angle of 45 degrees as the pattern for the first and the second photomasks can increase the density of the hole patterns.

[0035] The present invention uses a first and a second photomasks having two diagonally allocated square patterns that are rotated a fixed angle of 45 degrees to perform two exposure processes. Therefore, it is simpler than the conventional approach that uses optical proximity correction (OPC).

[0036] According to the present invention, during the exposure and development processes that are being performed on the wafer, the standard required by the product design is achieved. The yield and the productivity are thereby increased.

[0037] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.